IN THE CLAIMS

1. (currently amended): A circuit design method to control access pointers of different memory, which employs an (m+n)-bit read control signal circuit and an (m+n)-bit write control signal circuit to control the access pointers of a memory with 2^m-block, and each block has 2^n-register in order to perform buffer access of printers, comprising the following steps:

retrieving the previous addresses of the read and write pointers;

receiving a control signal from a data source;

analyzing the control signal to extract a transfer mode, an access mode, and [[a]] an access number;

determining the control signal circuit (r_ptr or w_ptr) according to the transfer mode and the access mode;

ransforming the access number to determine a memory block control circuit (r_ptr_f or w_ptr_f) and a register control circuit (r_ptr_1 or w_ptr_1);

setting the access pointers pointing to the corresponding memory addresses of the memory block control circuit and the register control circuit; and

performing [[the]] a data access of the corresponding memory addresses.

2. (original): In accordance with the method in claim 1, wherein the data source is a central processing unit.

3. (original): In accordance with the method in claim 1, wherein the control signal comprises the transfer mode, the access mode and the access number.

4. (original): In accordance with the method in claim 3, wherein the transfer mode comprises a parallel mode and a sequential mode.

5. (original): In accordance with the method in claim 3, wherein the access number is a decimal number.

6. (original): In accordance with the method in claim 1, wherein the control signal circuit comprises the read control signal circuit and the write control signal circuit.

7. (original): In accordance with the method in claim 1, wherein the transformation of the access number is to transform the number into an (m+n)-bit binary number.

8. (original): In accordance with the method in claim 1, wherein the memory block control circuit is determined by an m-bit binary number.

9. (original): In accordance with the method in claim 1, wherein the register control signal circuit is determined by an n-bit binary number.

10. (currently amended): In accordance with the method in claim [[1,]] 4, wherein the method further comprises the steps to determine the print mode control signal circuit set to perform the buffer access in said parallel mode or said sequential mode according to the access mode in the control signals.